Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

UG/PG DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL/MAY 2026

Third Semester

Electrical and Electronics Engineering

UEET24301 - DIGITAL LOGIC CIRCUITS

Regulations - 2024

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BTL*	*CO*	*Marks*
1.	Define Demorgan's Theorem.	L1	1	2
2.	Find the equivalent octal and decimal number for a given binary number 11010.	L1	1	2
3.	Draw a logic circuit for the truth table shown in figure.	L1	2	2

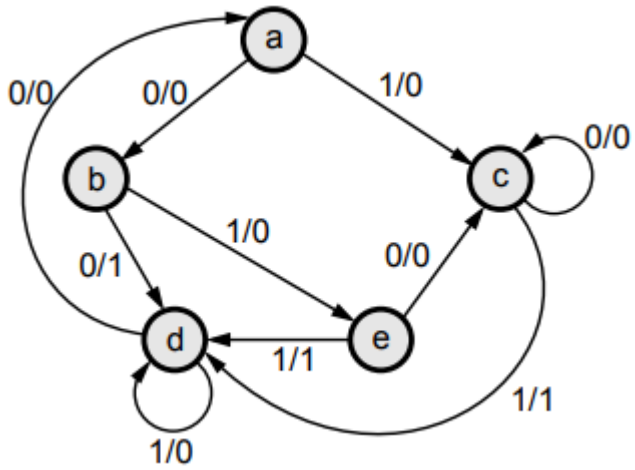
Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

4.		Compare between multiplexer and encoder.	L2	2	2
5.		Classify the different types of triggering signals used in synchronous sequential circuits.	L2	3	2
6.		Tell me the condition at which the two states are said to be equal.	L1	3	2
7.		Illustrate static 1 hazard with a neat waveform.	L2	4	2
8.		Recall the programmable logic devices.	L1	4	2
9.		Outline the different operators used in HDL.	L1	5	2
10.		Interpret the syntax of VHDL entity and architecture.	L2	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Reduce the given Boolean expression using K-map and implement the reduced expression using AOI logic. F (A, B, C, D) =∑m (0, 2, 3, 6, 7) + d (8, 10, 11, 15)	L2	1	16
			Or			
	b		Reduce the given Boolean expression using Quine McCluskey method. Y(a,b,c,d) = Σm (0,1,4,5,13,14,15)	L2	1	16
12.	a	i	Simplify a Full adder using two half adders with an OR gate.	L4	2	8
		ii	Analysis the half subtractor using 2:4 decoder.	L4	2	8
			Or			
	b	i	Contrast the 1:4 Demultiplexer using logic gates.	L4	2	8
		ii	Implement the given function using 8:1 multiplexer. Y= Σm (0,1,3,4,5,7,9,11,13,15)	L4	2	8

13.	a	i	Construct the SR latch using NOR gates and explain its four mode of operation with its truth table.	L3	3	8
		ii	Organize the given state diagram using state reduction technique.	L3	3	8



Or

	b		Development of a synchronous counter to count 0,1,.....7 using JK Flip Flop.	L3	3	16
14.	a		Design an asynchronous sequential circuit with two inputs x1 and x2 and one output Z. Initially, both inputs are equal to zero. When x1 or x2 becomes 1, the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state.	L4	4	16

Or

	b	i	Implement the combinational circuit with a PLA having 3 inputs, 4 product terms and 2 outputs for the functions. F1(A,B,C)= ∑ (0, 1, 2, 4) F2(A,B,C)=∑ (0, 5, 6, 7).	L4	4	10
		ii	Design a hazard free circuit for the given function Y = Σm(1,3,6,7).	L4	4	6
15.	a		Construct the digital logic circuit to subtract three binary bits using logic gates and also develop the VHDL code for the same.	L3	5	16

Or

	b		Apply an 8:1 multiplexer using basic logic gates and write the VHDL code for the developed model.	L3	5	16